During testing of the Flash EPROM cell 52, the bypass switch 50 is closed thereby bypassing transistors 46a-46n. This reduces the voltage observed at the cathode of the protective diode 38 by $n*V_t$. Thus, the margin erase voltage is given by:

$$V_{MP} = V_{bd} + V_t.$$

IN THE CLAIMS

Please amend the Claims as follows:

1. (AMENDED) A method of margin erasing memory cells in a testing procedure of a flash EPROM memory in an integrated circuit wherein said margin erasing uses charge pump circuitry to develop both a normal erase voltage used by an end user and a margin erase voltage used in said testing procedure.

4. (AMENDED) The method according to Claim 3 wherein said series connected voltage dropping components are diode connected NMOS transistors, PMOS transistors, native NMOS transistors or diodes.

14. (AMENDED) A method of margin erasing memory cells in a testing procedure of a flash EPROM memory in an integrated circuit wherein said margin erasing uses an internal charge pump circuit to develop both a normal erase voltage used by an end user and a margin erase voltage used in said testing procedure and wherein said margin erase

voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage.

16. (AMENDED) The method according to Claim 15 wherein said series connected voltage dropping components are diode connected NMOS transistors, PMOS transistors, native NMOS transistors or diodes.

26. AMENDED) A flash EPROM memory device comprising:

a charge pump circuit;

a protective diode having a cathode and an anode wherein said cathode of said protective diode is connected to said charge pump circuit;

a plurality of series connected voltage dropping devices wherein a drain of a first of said plurality of series connected voltage dropping devices is connected to said anode of said protective diode;

a bias current source connected to a source of a last of said plurality of series connected voltage dropping devices; and

a bypass switch to bypass one or more of said series connected voltage dropping devices.

27. (AMENDED) The method according to Claim 26 wherein said series connected voltage dropping devices are diode connected NMOS transistors, PMOS transistors, native NMOS transistors or diodes.